

Deep Learning for Temporal Logics

Frederik Schmitt, Christopher Hahn, Jens U. Kreber,
Markus N. Rabe, Bernd Finkbeiner

6th Conference on Artificial Intelligence and Theorem Proving

September 6, 2021



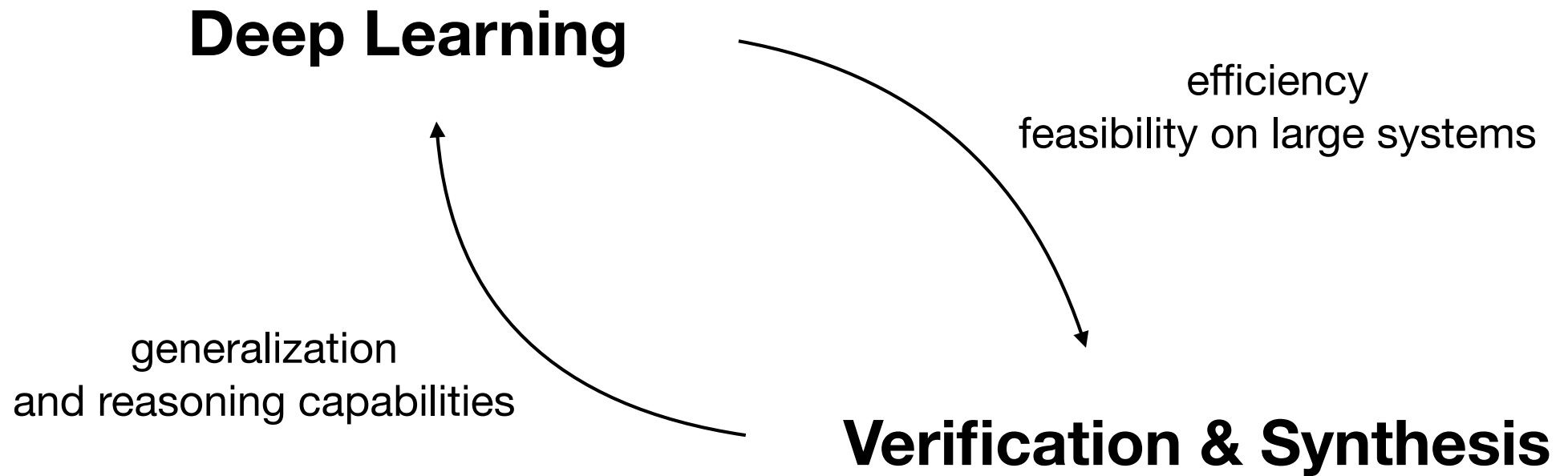
CISPA
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INFORMATION SECURITY



UNIVERSITÄT
DES
SAARLANDES

Google Research

Deep Learning for Formal Methods



Examples of Related Work

NeuroSAT

Selsam, D., Lamm, M., Bünz, B., Liang, P., de Moura, L., Dill, D.L.: Learning a SAT Solver from Single-Bit Supervision. ICLR 2019

FastSMT

Balunović, M., Bielik, P., Vechev, M.: Learning to Solve SMT Formulas. NeurIPS 2018

DeepHOL

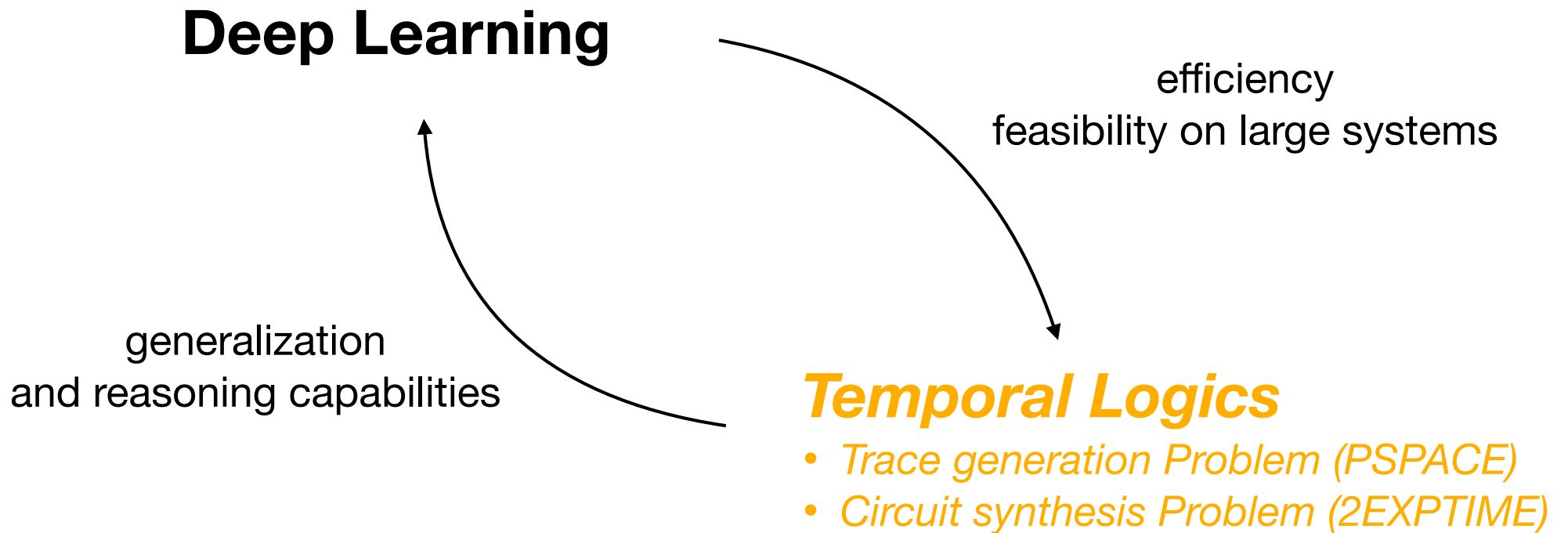
Bansal, K., Loos, S.M., Rabe, M.N., Szegedy, C., Wilcox, S.: HOList: An Environment for Machine Learning of Higher-Order Theorem Proving. ICML 2019

DeepMath

Alemi, A. A., Chollet, F., Een, N., Irving, G., Szegedy, C., Urban, J.: DeepMath: Deep Sequence Models for Premise Selection. NeurIPS 2016

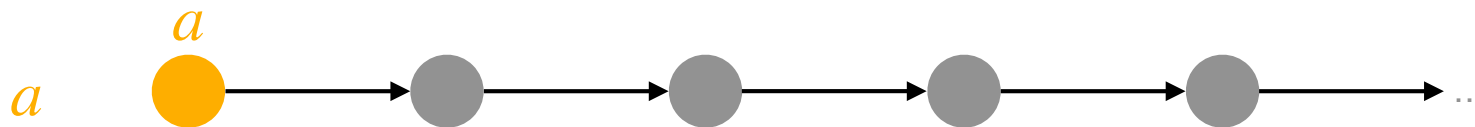
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Deep Learning for Temporal Logics



Linear-time Temporal Logic (LTL)¹

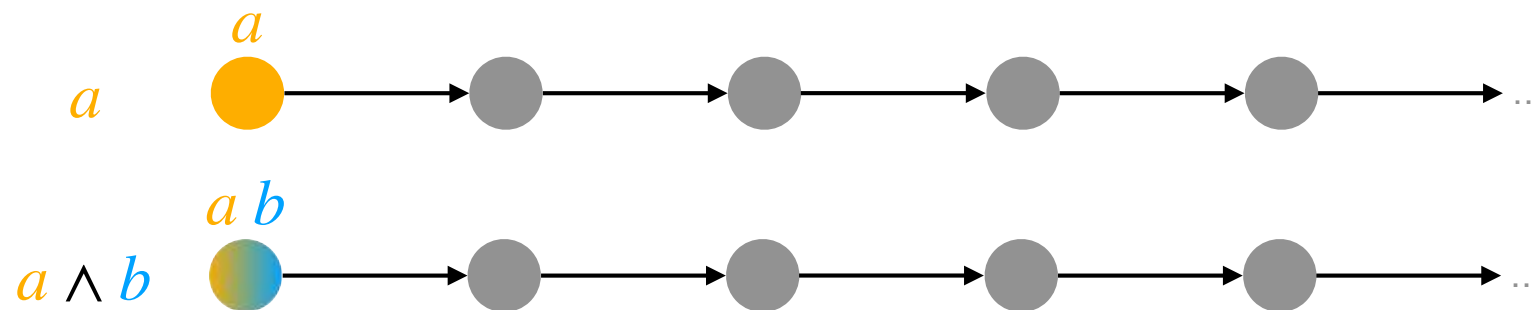
$\varphi, \psi ::= a \mid \text{true} \mid \neg\varphi \mid \varphi \wedge \psi \mid \bigcirc\varphi \mid \varphi \cup \psi$ where $a \in AP$



¹ Pnueli, A.: The Temporal Logic of Programs. 18th Annual Symposium on Foundations of Computer Science, Providence, Rhode Island, USA, 1977

Linear-time Temporal Logic (LTL)¹

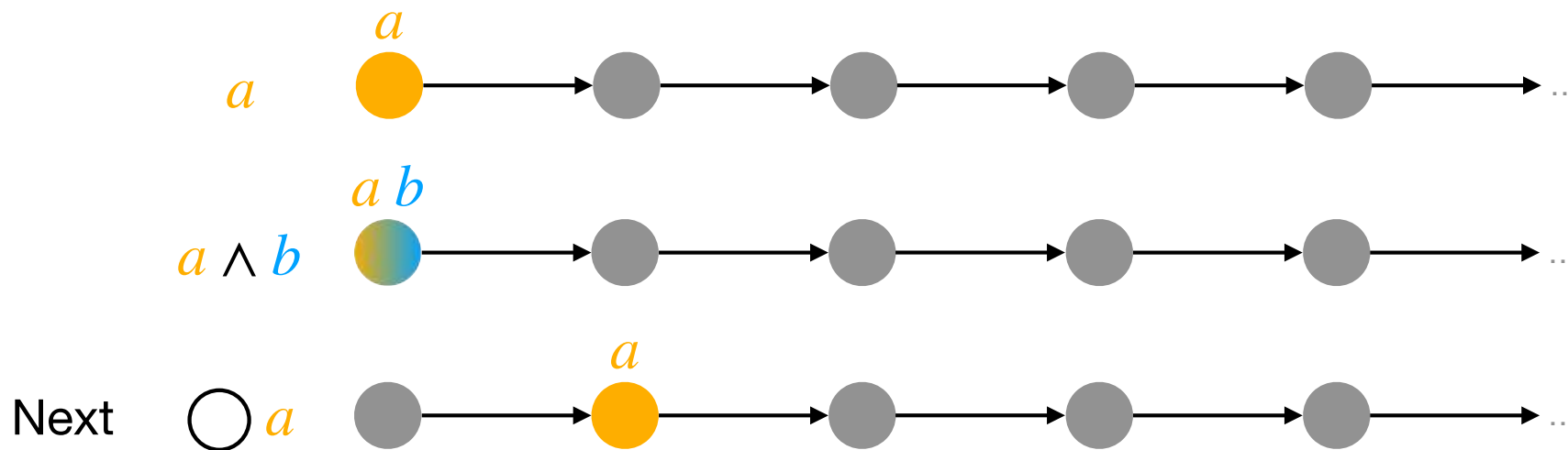
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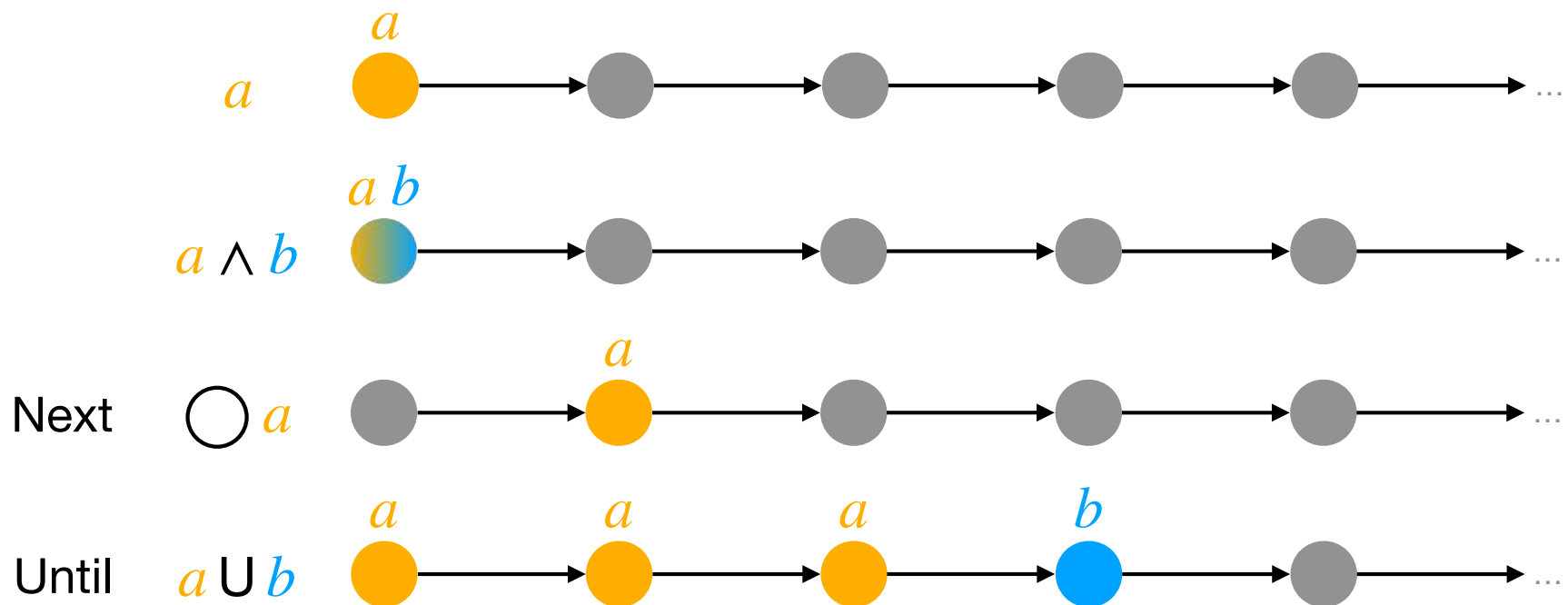
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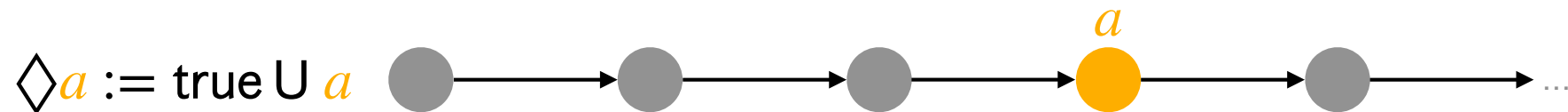
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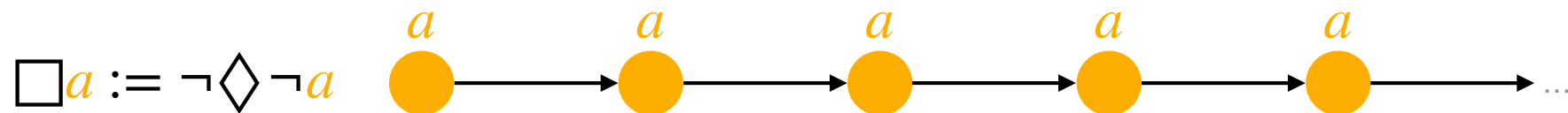
¹ Pnueli, A.: The Temporal Logic of Programs. 18th Annual Symposium on Foundations of Computer Science, Providence, Rhode Island, USA, 1977

Linear-time Temporal Logic (LTL)¹

Eventually



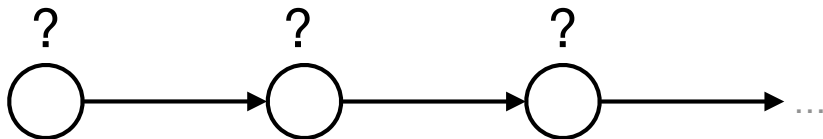
Globally



¹ Pnueli, A.: The Temporal Logic of Programs. 18th Annual Symposium on Foundations of Computer Science, Providence, Rhode Island, USA, 1977

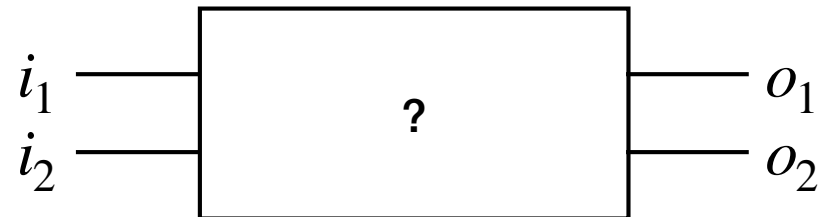
Part 1: Trace Generation

Trace $\pi \models$ LTL Formula φ



Part 2: Circuit Synthesis

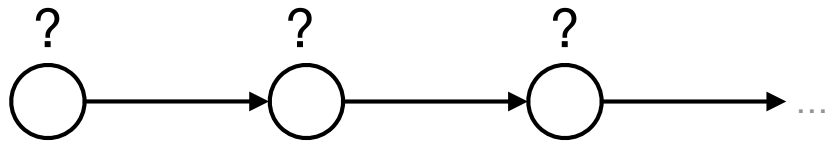
Circuit $C \models$ LTL Specification φ



Hahn, C., S., F., Kreber, J.U., Rabe, M.N., Finkbeiner, B.: Teaching Temporal Logics to Neural Networks. ICLR 2021
S., F., Hahn, C., Rabe, M.N., Finkbeiner, B.: Neural Circuit Synthesis from Specification Patterns. arXiv Preprint 2021

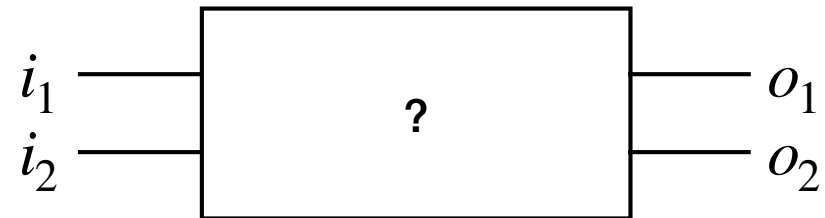
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Part 2: Circuit Synthesis

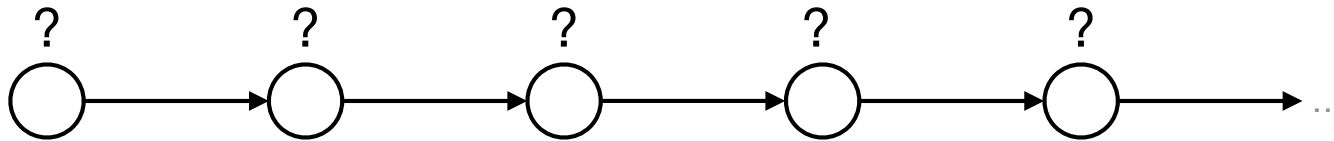
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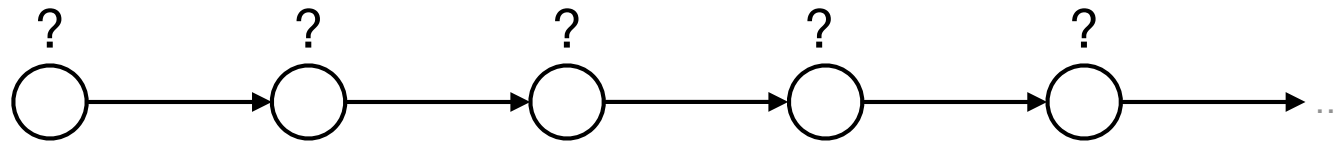
Trace Generation Problem

$$(a \cup (b \wedge c)) \wedge (a \cup (\neg b \wedge c)) \wedge (a \cup (\neg b \wedge \neg c))$$



Trace Generation Problem

$$(a \text{ U } (b \wedge c)) \wedge (a \text{ U } (\neg b \wedge c)) \wedge (a \text{ U } (\neg b \wedge \neg c))$$

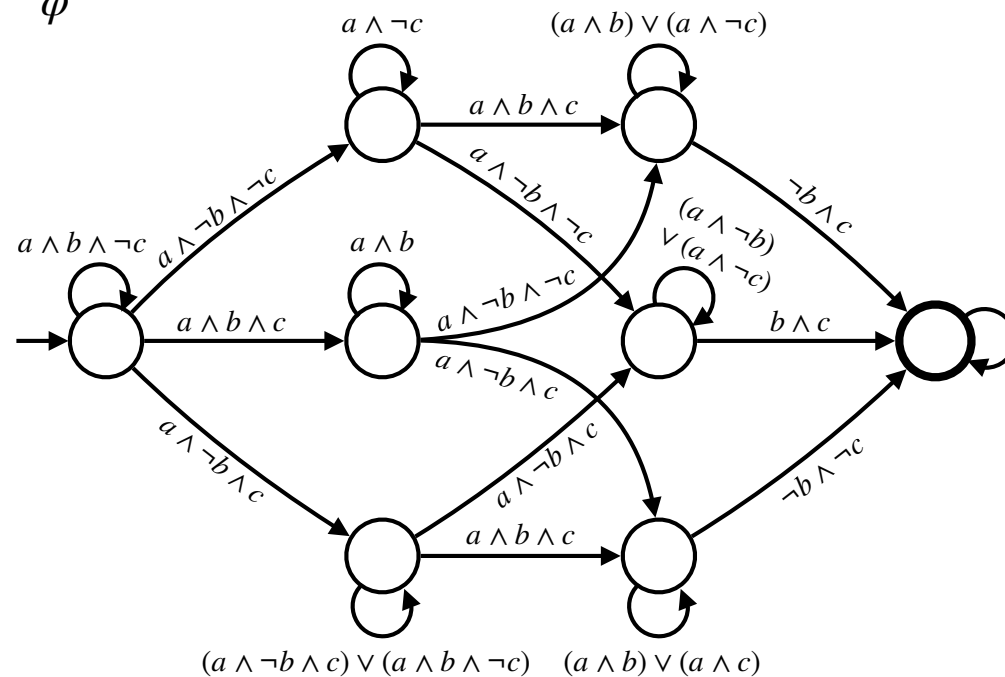


The LTL Trace Generation Problem is PSPACE-complete.

Classic Trace Generation

$$\varphi = (a \cup (b \wedge c)) \wedge (a \cup (\neg b \wedge c)) \wedge (a \cup (\neg b \wedge \neg c))$$

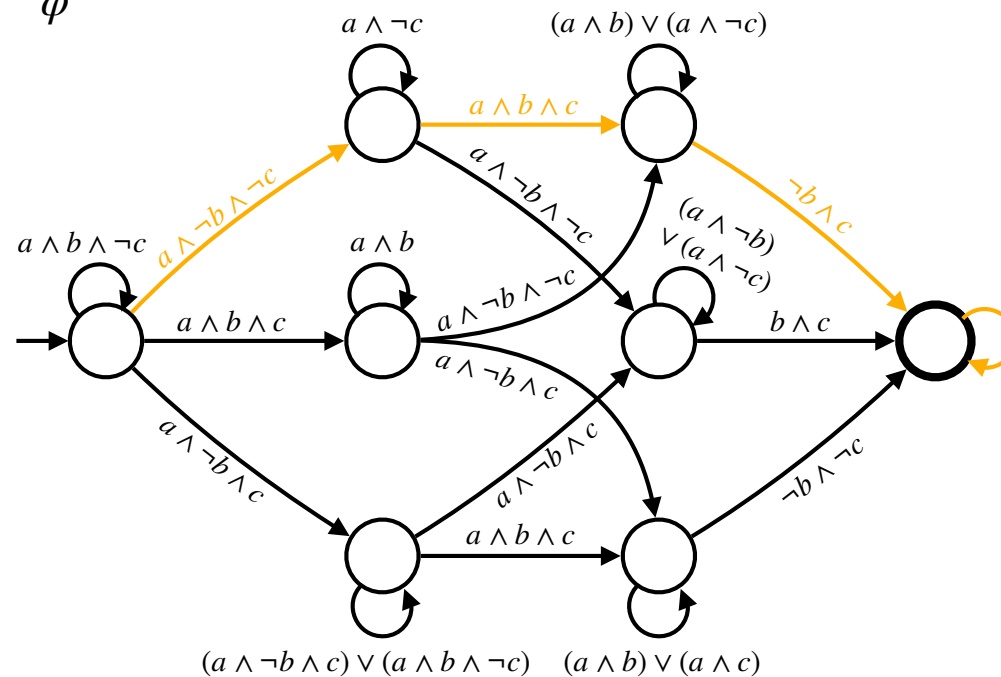
Büchi Automaton A_φ



Classic Trace Generation

$$\varphi = (a \cup (b \wedge c)) \wedge (a \cup (\neg b \wedge c)) \wedge (a \cup (\neg b \wedge \neg c))$$

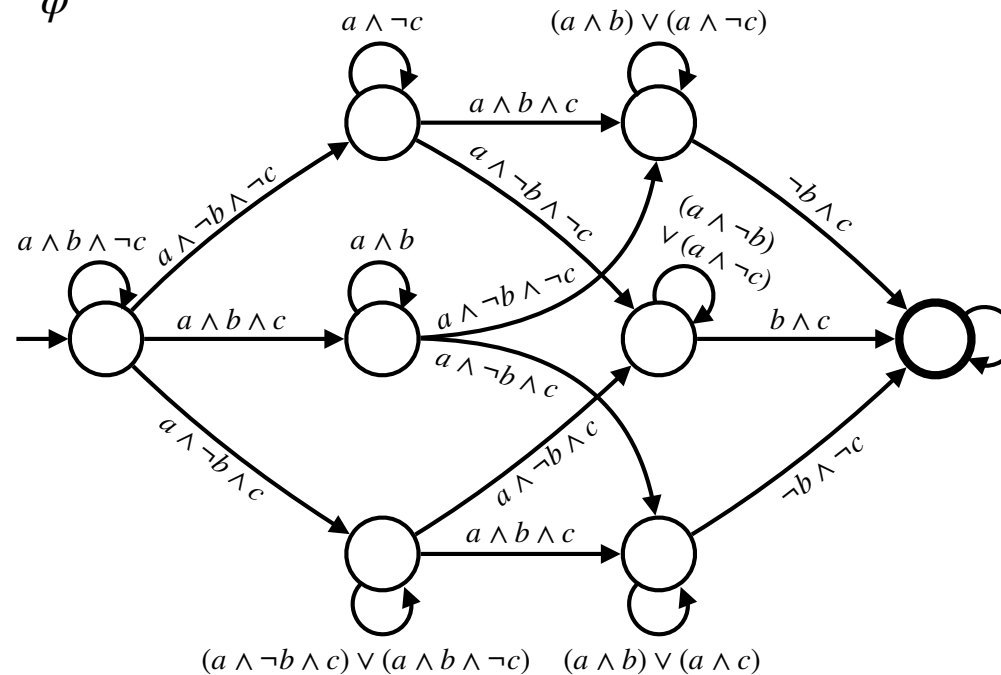
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Classic Trace Generation

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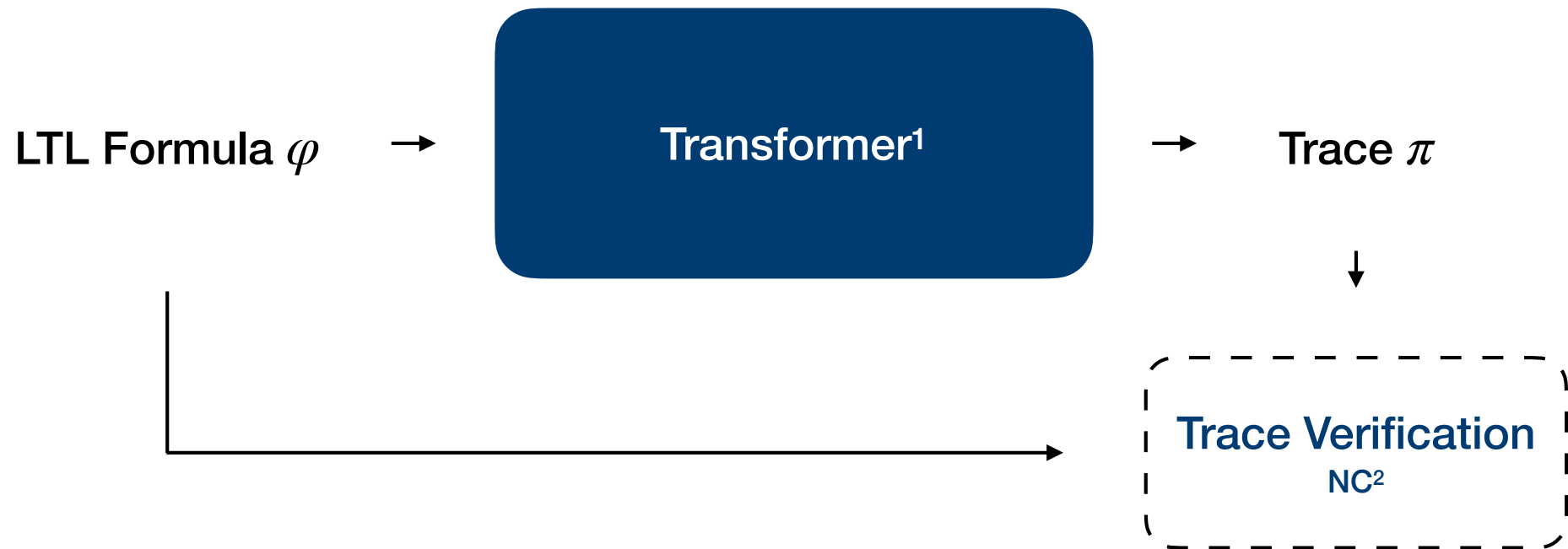
The number of states can be exponential in $|\varphi|$.

Neural Trace Generation



¹ Vaswani, A., Shazeer, N., Parmar, N., Uszkoreit, J., Jones, L., Gomez, A.N., Kaiser, L., Polosukhin, I.: Attention is All you Need. NeurIPS 2017

Neural Trace Generation



¹ Vaswani, A., Shazeer, N., Parmar, N., Uszkoreit, J., Jones, L., Gomez, A.N., Kaiser, L., Polosukhin, I.: Attention is All you Need. NeurIPS 2017

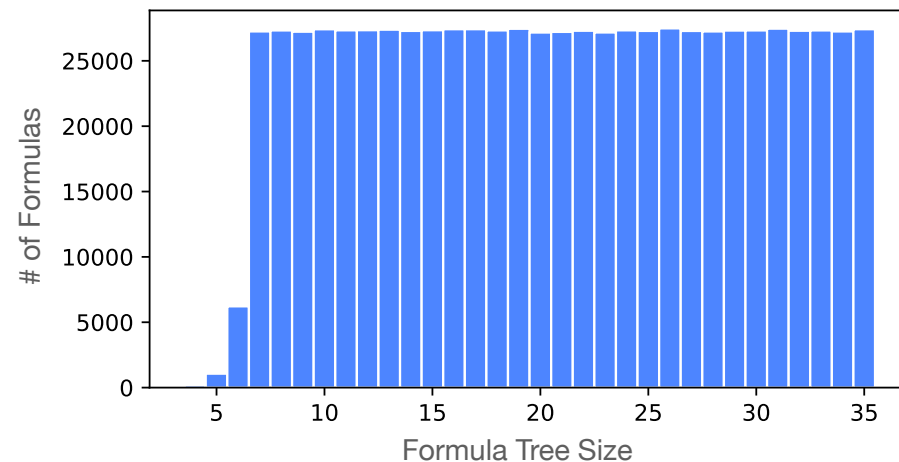
² Kuhtz, L., Finkbeiner, B.: LTL Path Checking is Efficiently Parallelizable. ICALP 2009

Neural Trace Generation

Datasets

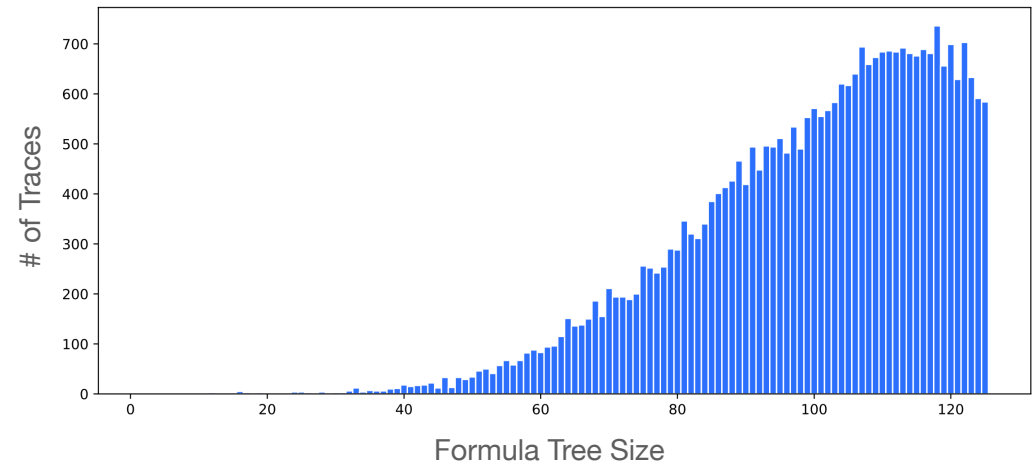
LTLRandom35

- 1,000,000 formula-trace pairs
- Generated randomly
- Uniformly distributed in formula size



LTLPattern126

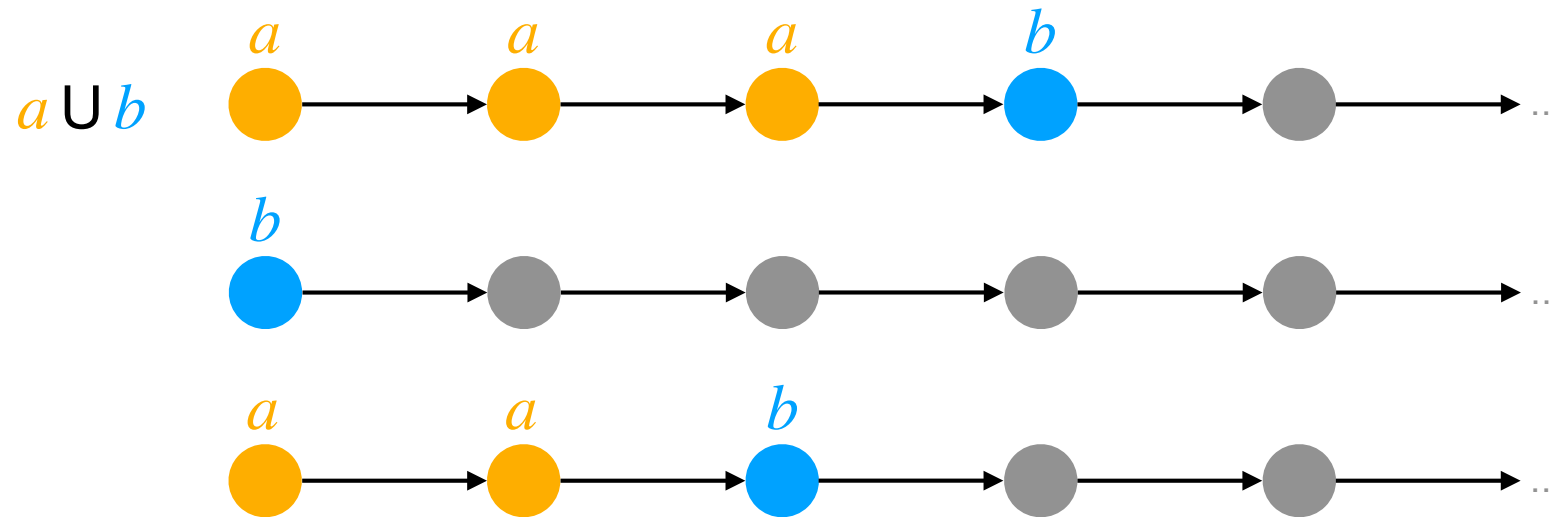
- 1,664,487 formula-trace pairs
- Constructed from formula patterns¹
- Conjunctions of patterns are hard to solve



¹ Dwyer, M. B., Avrunin, G.S., Corbett, J.C.: Property Specification Patterns for Finite-State Verification. 2017

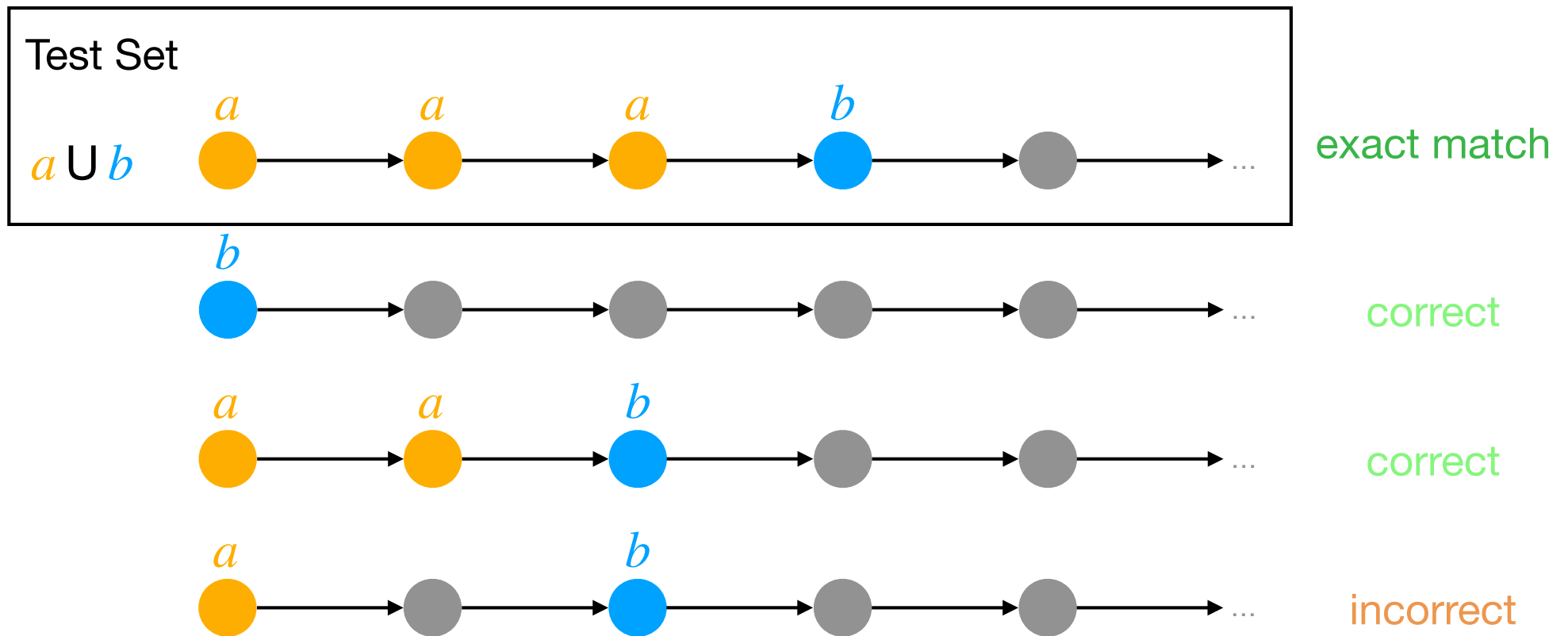
Neural Trace Generation

Performance Measures



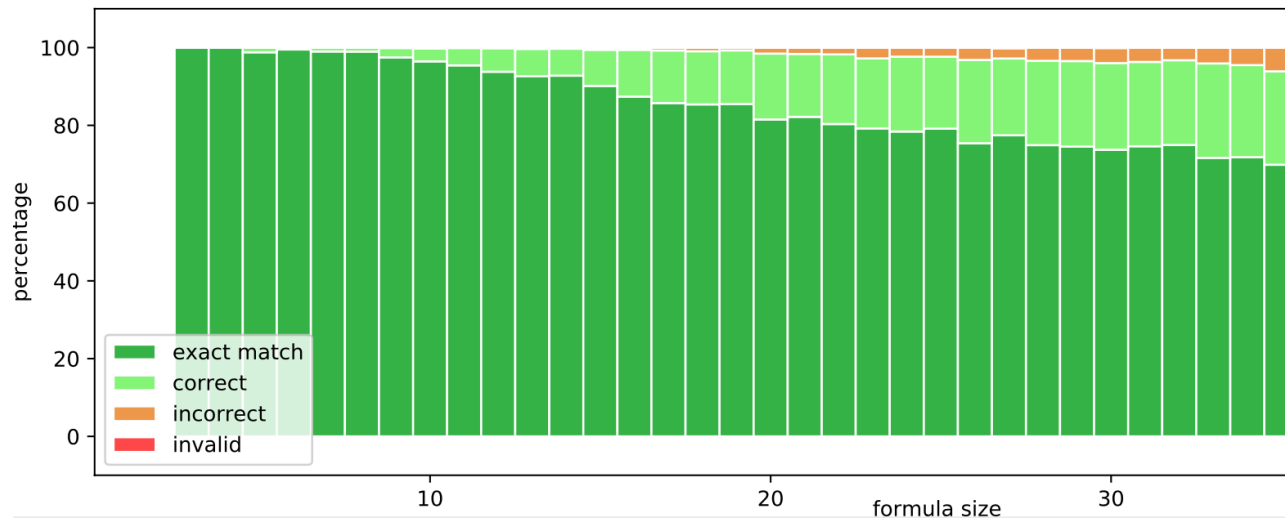
Neural Trace Generation

Performance Measures



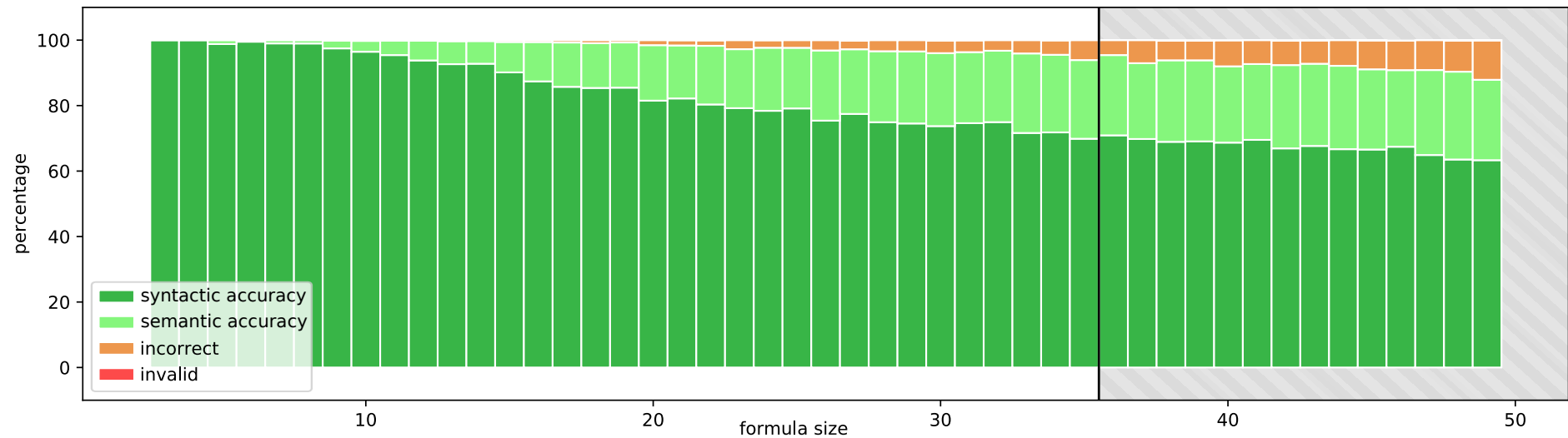
Neural Trace Generation

Results - LTLRandom35



Neural Trace Generation

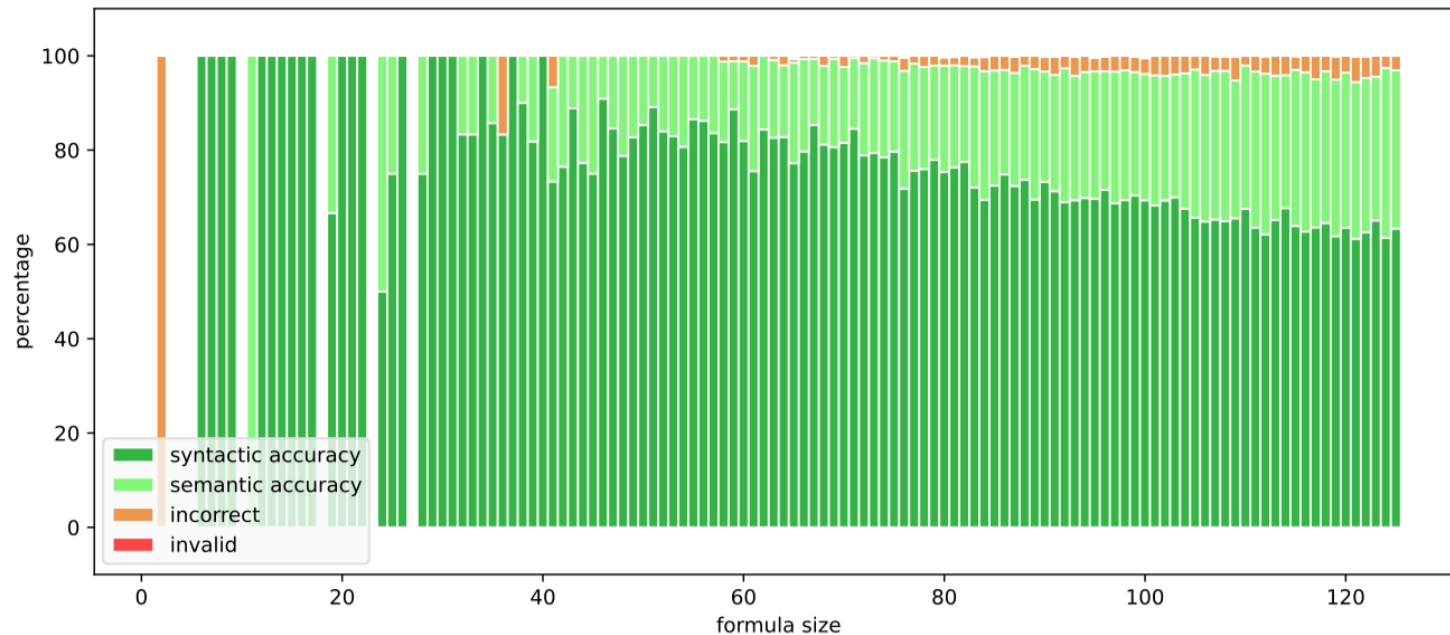
Results - LTLRandom35



Tree positional encoding: Shiv, V. L. and Quirk, C.: Novel positional encodings to enable tree-based transformers. NeurIPS 2019

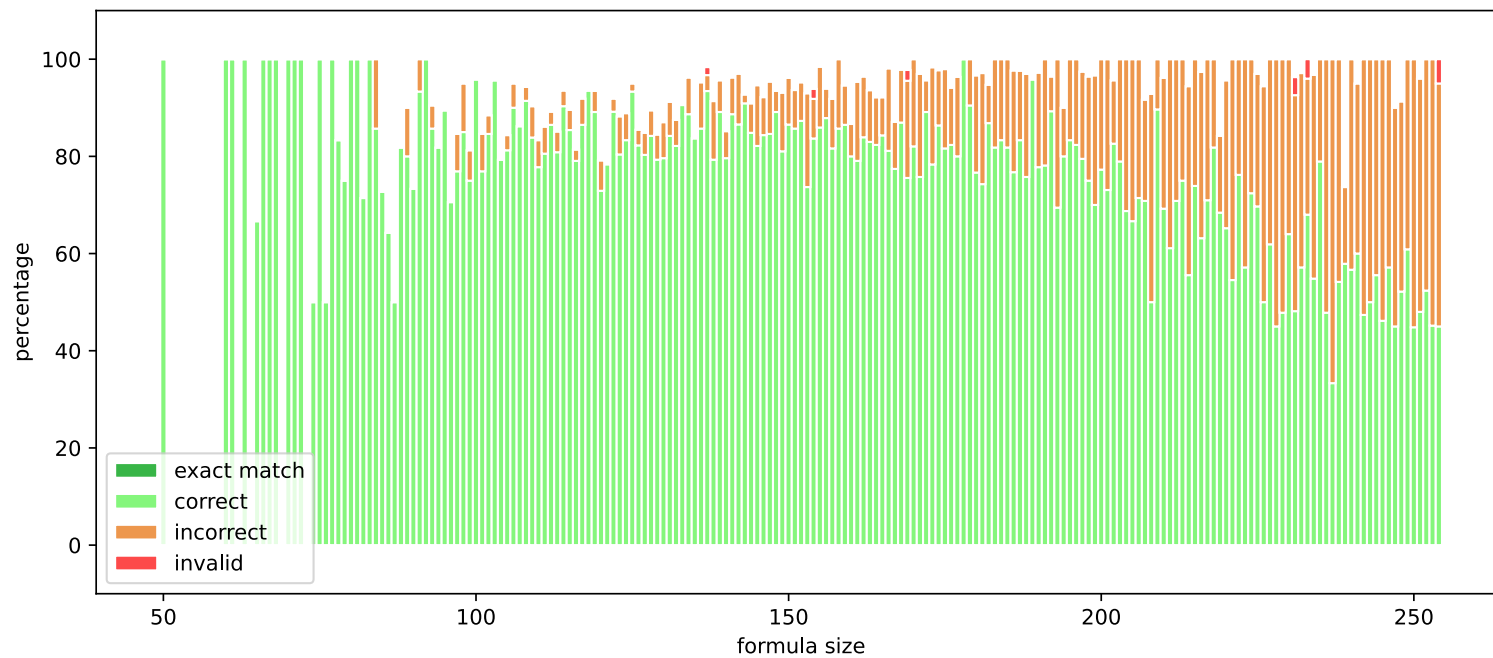
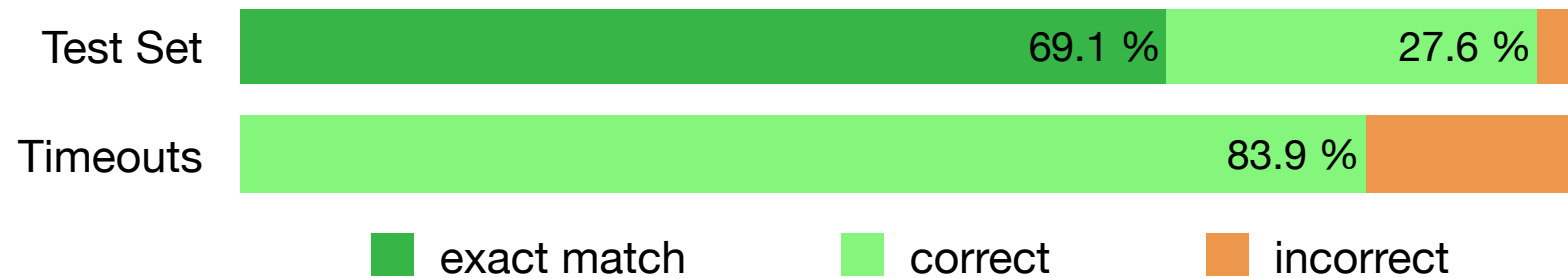
Neural Trace Generation

Results - LTLPattern126



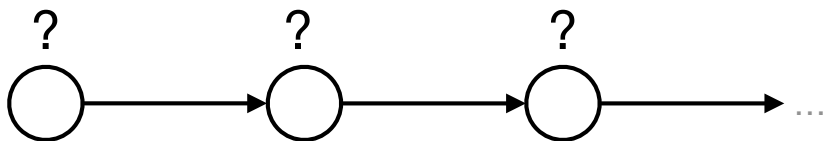
Neural Trace Generation

Results - LTLPattern126



Part 1: Trace Generation

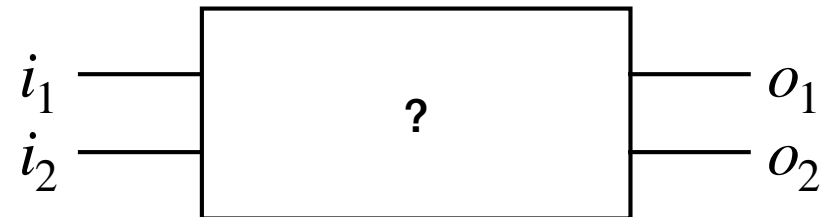
Trace $\pi \models$ LTL Formula φ



- Semantic generalization
- Generalization to larger formulas with tree positional encoding

Part 2: Circuit Synthesis

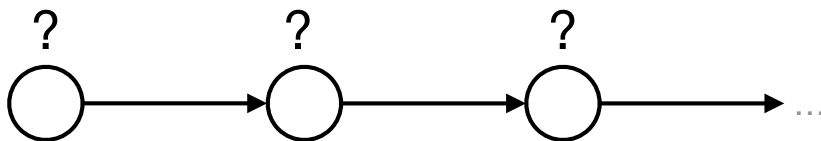
Circuit $C \models$ LTL Specification φ



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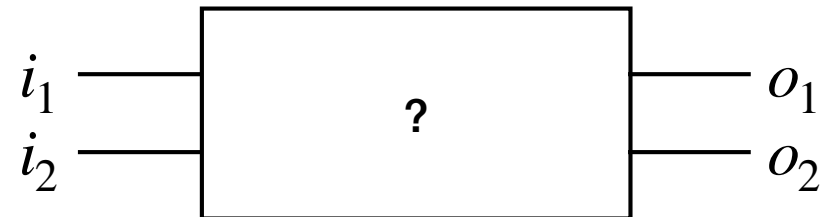
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Church's Problem



“Given a requirement which a circuit is to satisfy (...). The synthesis problem is then to find recursion equivalences representing a circuit that satisfies the given requirement (or alternatively, to determine that there is no such circuit).”

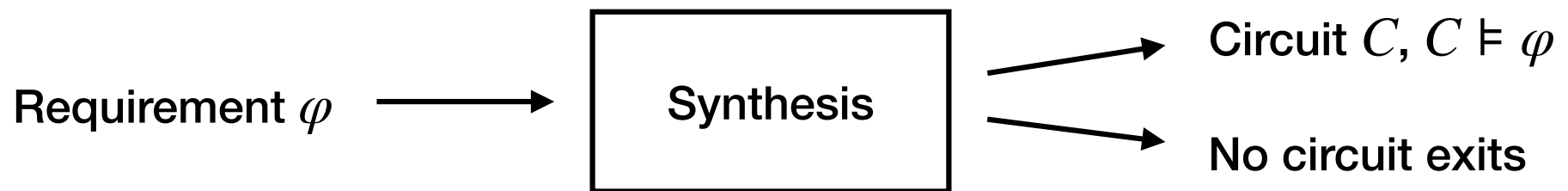
Alonzo Church, 1957

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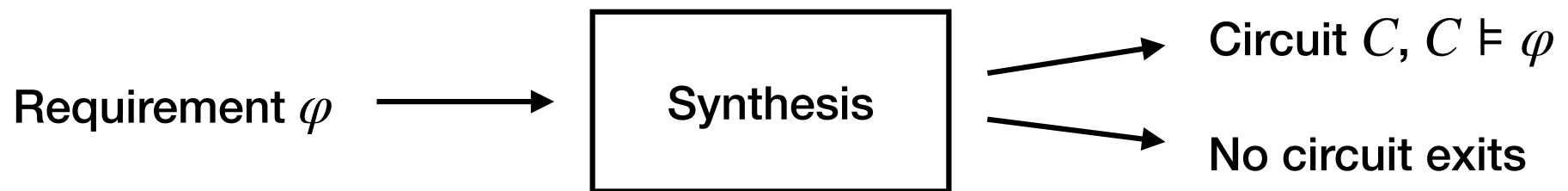


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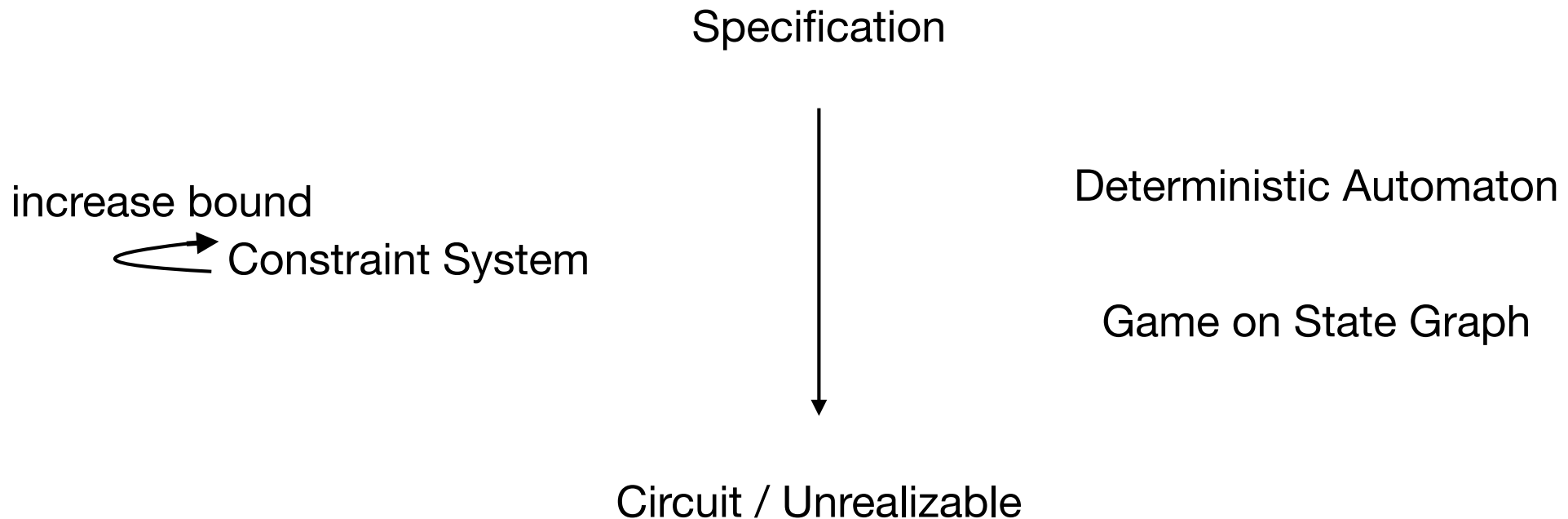
Alonzo Church, 1957



Classic LTL Synthesis

Bounded Synthesis¹

Game-based Synthesis²



The LTL Synthesis Problem is 2EXPTIME-complete³.

¹ Schewe, S., Finkbeiner, B.: Bounded Synthesis. ATVA 2007

² Büchi, J.R., Landweber, L.H.: Solving Sequential Conditions by Finite-State Strategies. Transactions of the American Mathematical Society Vol. 183 1969

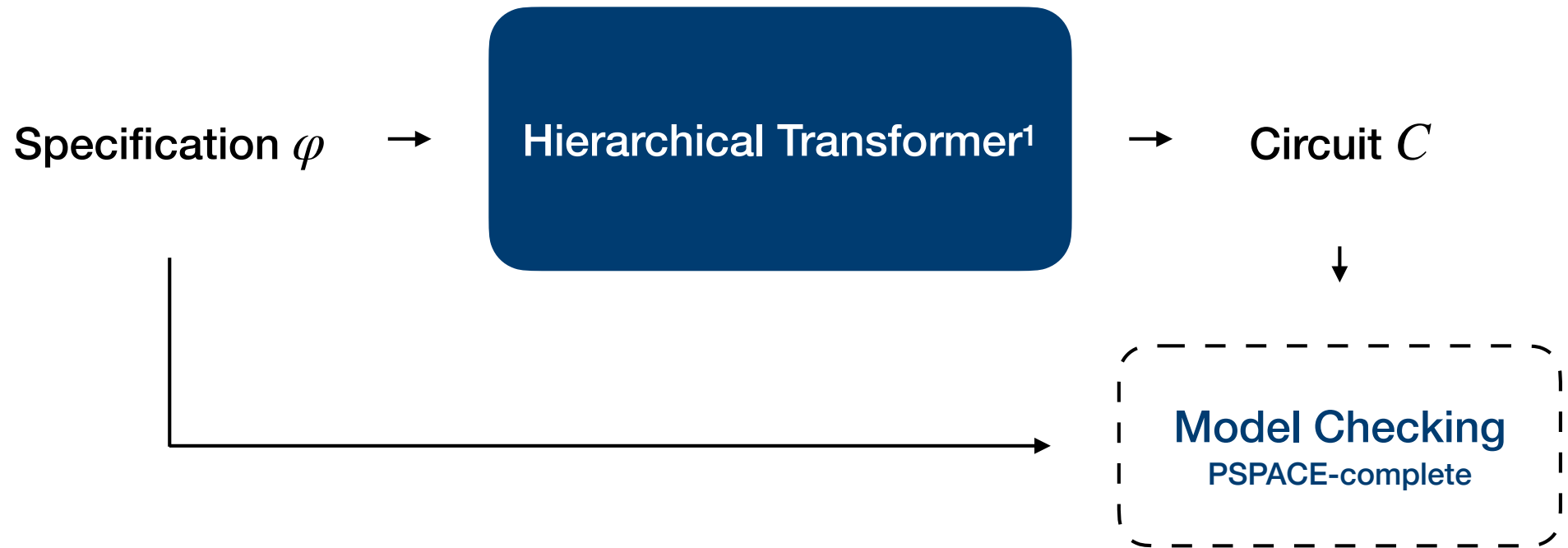
³ Pnueli, A., Rosner, R.: On the Synthesis of a Reactive Module. POPL 1989

Neural LTL Synthesis



¹ Li, W., Yu, L., Wu, Y., Paulson, L.C.: IsarStep: a Benchmark for High-level Mathematical Reasoning. ICLR 2021

Neural LTL Synthesis



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Neural LTL Synthesis

Data Generation from Specification Patterns

$\square(r_1 \Rightarrow \diamond g_1)$	Response	$AP = I \cup O$
$\wedge \square(r_2 \Rightarrow \diamond g_2)$	Response	$I = \{r_1, r_2\}$
$\wedge \square \neg(g_1 \wedge g_2)$	Mutual Exclusion	$O = \{g_1, g_2\}$

Neural LTL Synthesis

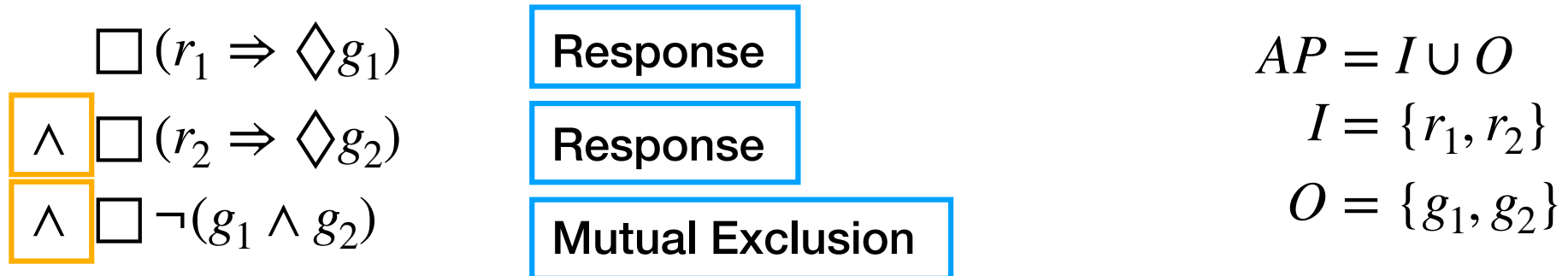
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Conjunctions of smaller guarantees

Neural LTL Synthesis

Data Generation from Specification Patterns



Conjunctions of smaller guarantees

Frequent patterns

Neural LTL Synthesis

Data Generation from Specification Patterns

$\square(r_1 \Rightarrow \bigcirc(\neg g_2 \cup g_1))$	Prioritized Response
$\wedge \square(r_2 \Rightarrow \blacklozenge g_2)$	Response
$\wedge \square \neg(g_1 \wedge g_2)$	Mutual Exclusion

$$AP = I \cup O$$

$$I = \{r_1, r_2\}$$

$$O = \{g_1, g_2\}$$

Conjunctions of smaller guarantees

Frequent patterns

Neural LTL Synthesis

Data Generation from Specification Patterns

$\square \diamond \neg r_1$	Infinately Often $\neg r_1$
\Rightarrow	
$\square (r_1 \Rightarrow \bigcirc (\neg g_2 \cup g_1))$	Prioritized Response
$\wedge \square (r_2 \Rightarrow \diamond g_2)$	Response
$\wedge \square \neg (g_1 \wedge g_2)$	Mutual Exclusion

$$AP = I \cup O$$

$$I = \{r_1, r_2\}$$

$$O = \{g_1, g_2\}$$

Conjunctions of smaller guarantees

Frequent patterns

Assumptions

Neural LTL Synthesis

Data Generation from Specification Patterns

$\square \diamond \neg r_1$	Infinately Often $\neg r_1$
\Rightarrow	
$\square (r_1 \Rightarrow \bigcirc (\neg g_2 \cup g_1))$	Prioritized Response
$\wedge \square (r_2 \Rightarrow \diamond g_2)$	Response
$\wedge \square \neg (g_1 \wedge g_2)$	Mutual Exclusion

$AP = I \cup O$
 $I = \{r_1, r_2\}$
 $O = \{g_1, g_2\}$

Conjunctions of smaller guarantees

Frequent patterns

Assumptions

assumption₁ \wedge ... \wedge assumption_m \Rightarrow guarantee₁ \wedge ... \wedge guarantee_n

Neural LTL Synthesis

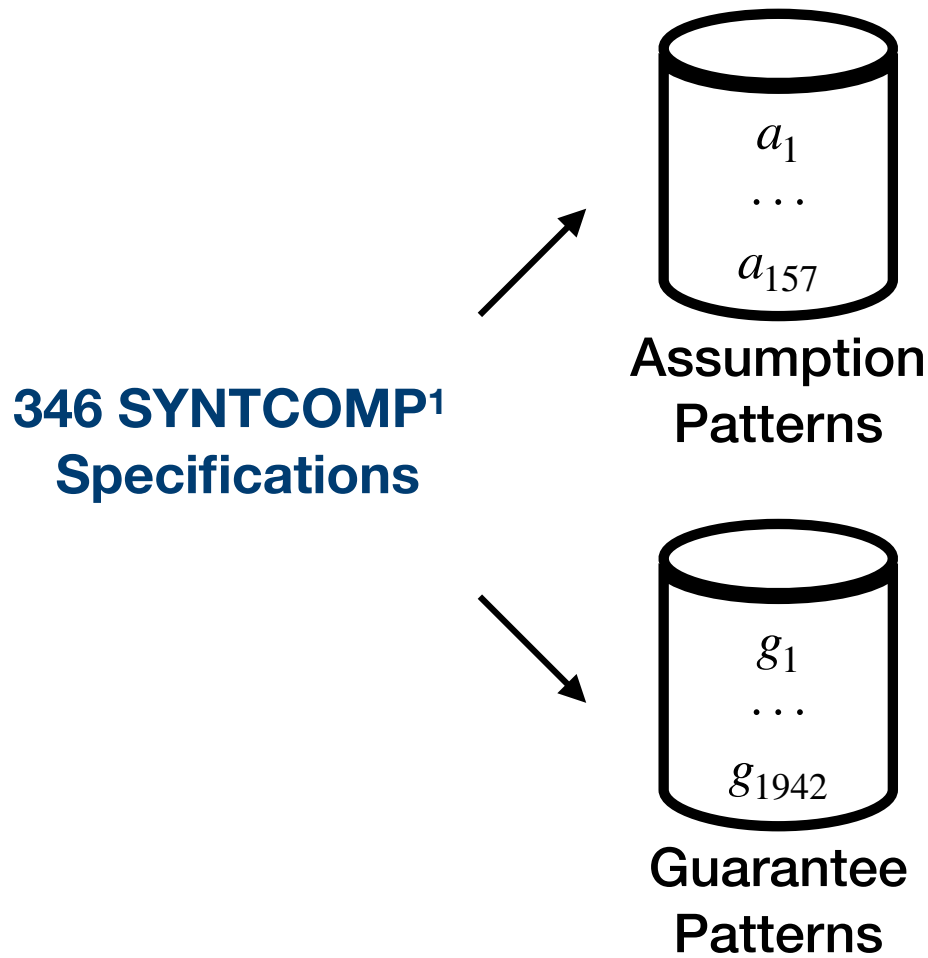
Data Generation from Specification Patterns

346 SYNTCOMP¹
Specifications

¹ <http://www.syntcomp.org>

Neural LTL Synthesis

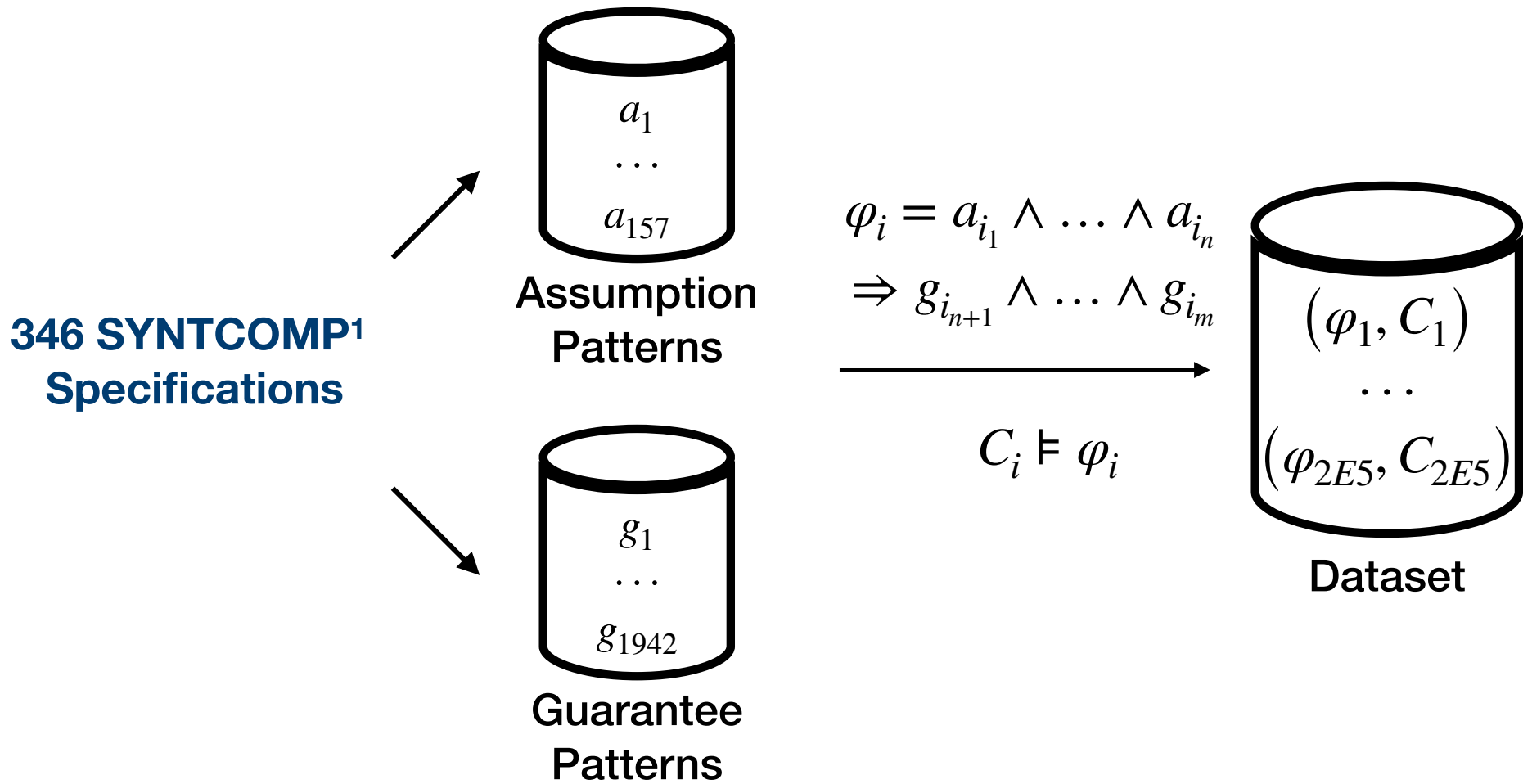
Data Generation from Specification Patterns



¹ <http://www.syntcomp.org>

Neural LTL Synthesis

Data Generation from Specification Patterns



¹ <http://www.syntcomp.org>

Neural LTL Synthesis

Hierarchical Transformer¹

AIGER Circuit C



Hierarchical Transformer

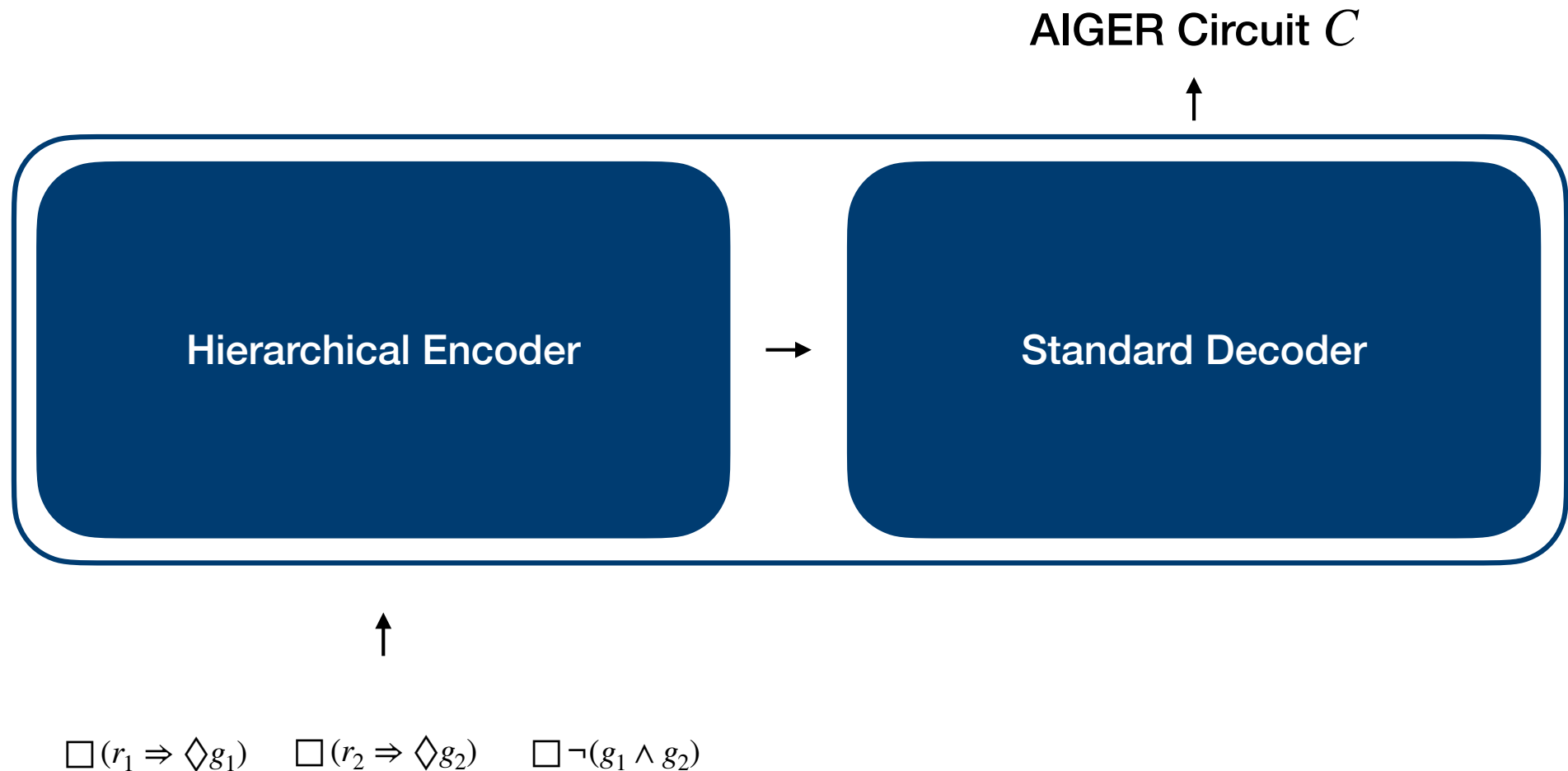


$\Box(r_1 \Rightarrow \Diamond g_1)$ $\Box(r_2 \Rightarrow \Diamond g_2)$ $\Box \neg(g_1 \wedge g_2)$

¹ Li, W., Yu, L., Wu, Y., Paulson, L.C.: IsarStep: a Benchmark for High-level Mathematical Reasoning. ICLR 2021

Neural LTL Synthesis

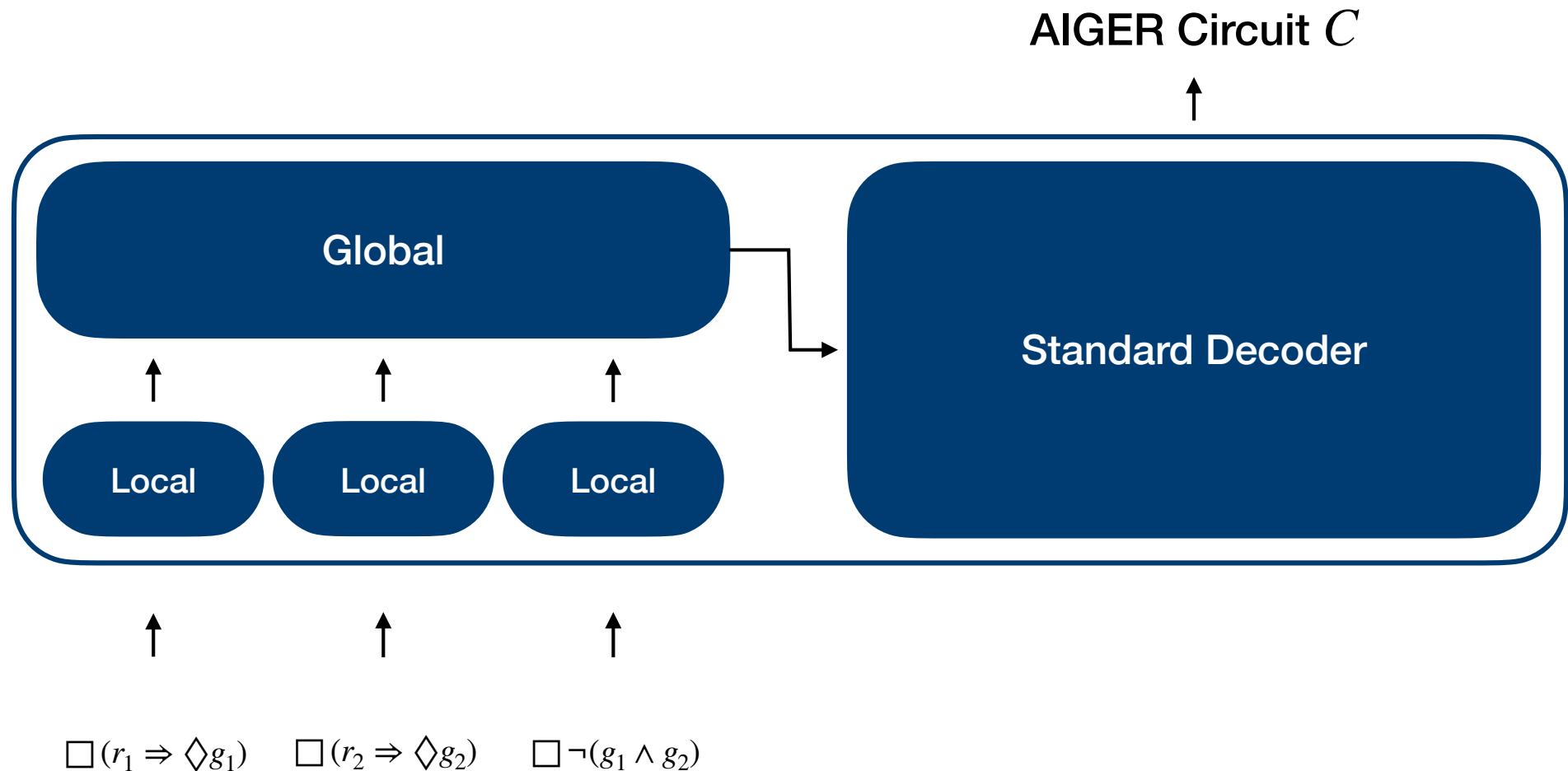
Hierarchical Transformer¹



¹ Li, W., Yu, L., Wu, Y., Paulson, L.C.: IsarStep: a Benchmark for High-level Mathematical Reasoning. ICLR 2021

Neural LTL Synthesis

Hierarchical Transformer¹

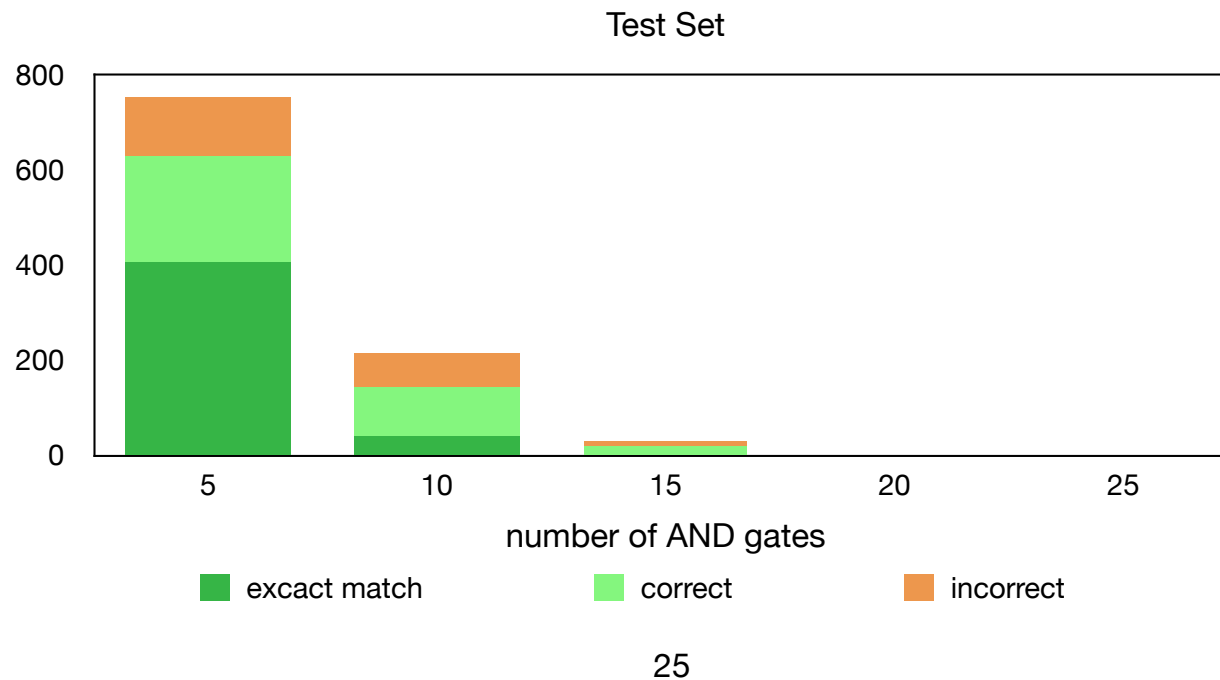


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Neural LTL Synthesis Results

Test Set

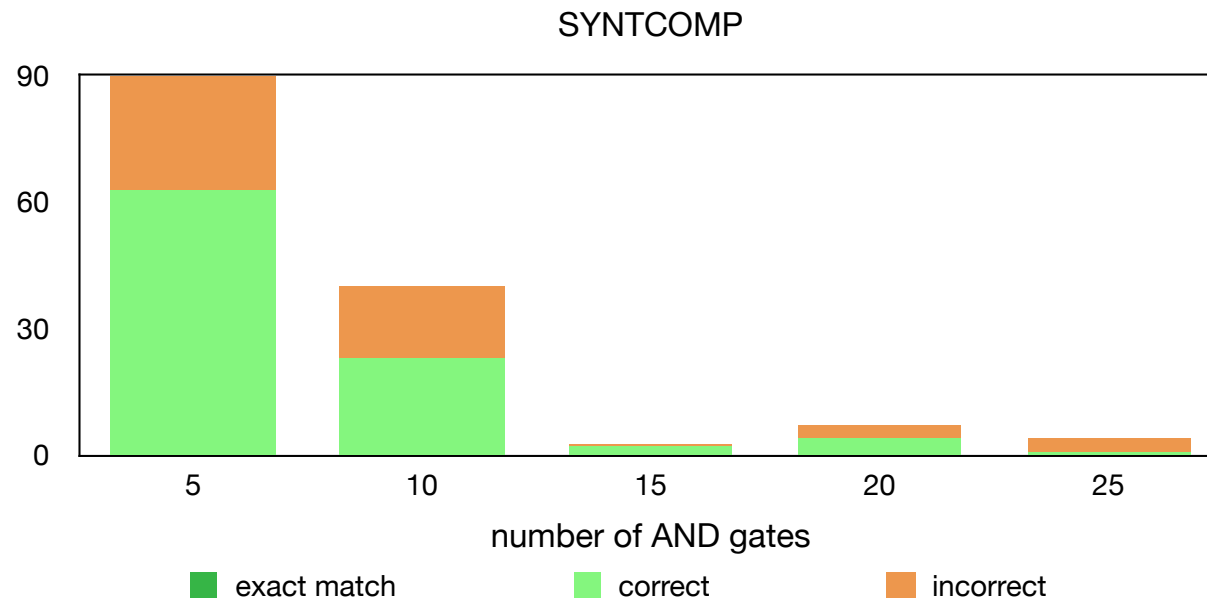
	Beam Size 1	Beam Size 4	Beam Size 8	Beam Size 16
Test Set	53.6	70.4	75.8	79.9



Neural LTL Synthesis Results

SYNTCOMP¹

	Beam Size 1	Beam Size 4	Beam Size 8	Beam Size 16
Test Set	53.6	70.4	75.8	79.9
SYNTCOMP	51.9	60.0	63.6	66.8

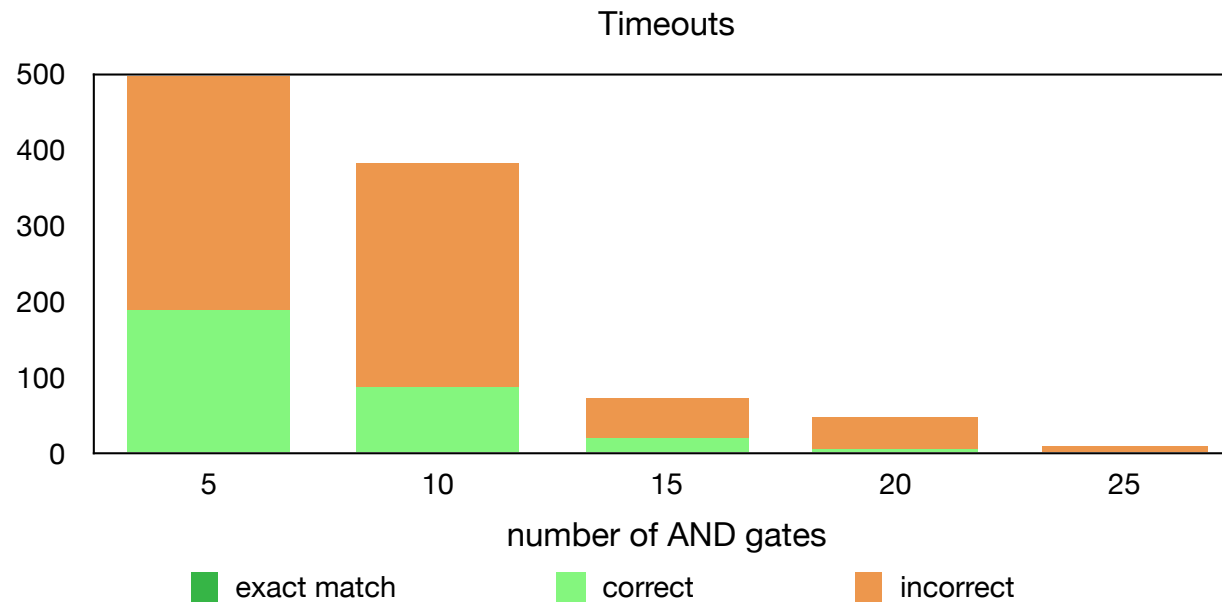


¹ <http://www.syntcomp.org>

Neural LTL Synthesis Results

Timeouts

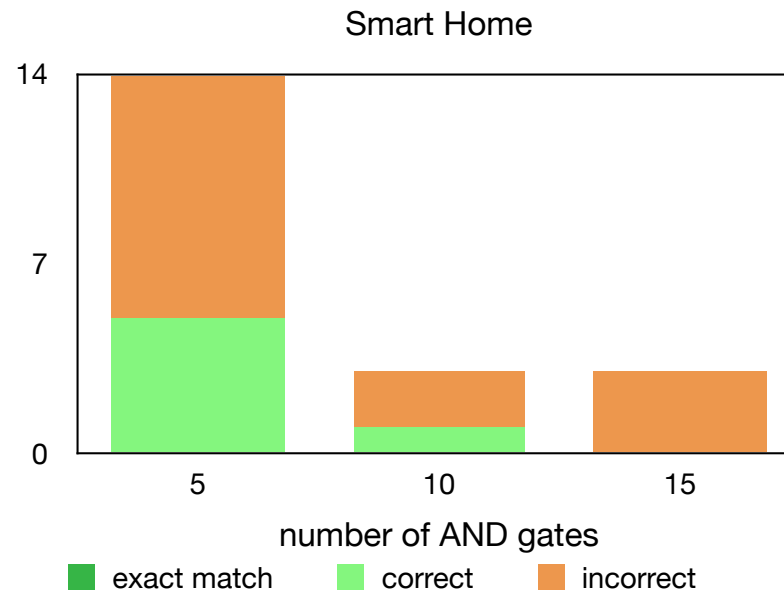
	Beam Size 1	Beam Size 4	Beam Size 8	Beam Size 16
Test Set	53.6	70.4	75.8	79.9
SYNTCOMP	51.9	60.0	63.6	66.8
Timeouts	11.7	21.1	25.9	30.1



Neural LTL Synthesis Results

Smart Home¹

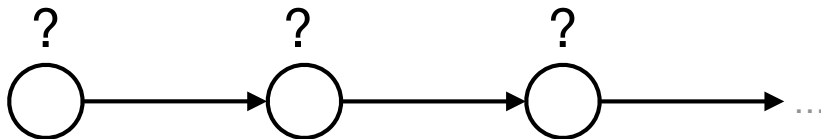
	Beam Size 1	Beam Size 4	Beam Size 8	Beam Size 16
Test Set	53.6	70.4	75.8	79.9
SYNTCOMP	51.9	60.0	63.6	66.8
Timeouts	11.7	21.1	25.9	30.1
Smart Home	22.9	31.4	44.8	40.0



¹ J.A.R.V.I.S. TSL/TLSF Benchmark Suite, 2021.

Part 1: Trace Generation

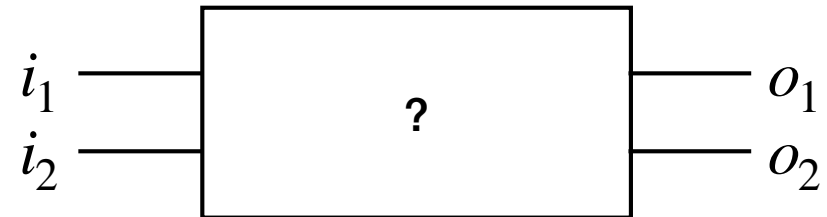
Trace $\pi \models$ LTL Formula φ



- Semantic generalization
- Generalization to larger formulas with tree positional encoding

Part 2: Circuit Synthesis

Circuit $C \models$ LTL Specification φ

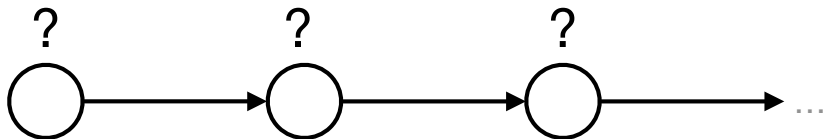


- Circuit synthesis end-to-end
- Generalizes to SYNTCOMP benchmarks

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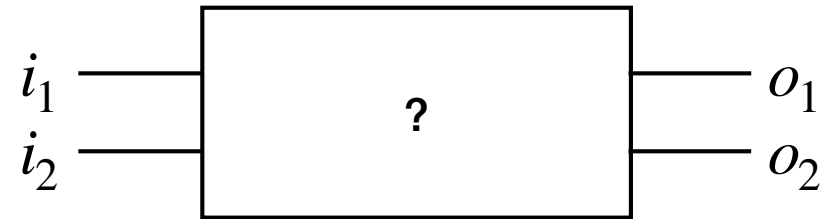
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- Generalization to larger formulas with tree positional encoding

Part 2: Circuit Synthesis

Circuit $C \models$ LTL Specification φ



- Circuit synthesis end-to-end
- Generalizes to SYNTCOMP benchmarks

With deep learning new types of fast algorithms for verification and synthesis can be developed.

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